Glomation

Embedded Single Board Computer

GESBC-9G25/35

User's Manual

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Chapter 1 – Introducing the GESBC-9G25/35 Single Board Computer

GESBC-9G25/35 Overview

The GESBC-9G25/35 is a low cost compact sized single board computer (SBC) based on Atmel AT91SAM9G25/35 processor. With a large peripheral set targeted to a variety of applications, the GESBC-9G25/35 is well suited for industrial controls, digital media servers, audio jukeboxes, thin clients, set-top boxes, point-of-sale terminals, biometric security systems, and GPS devices.

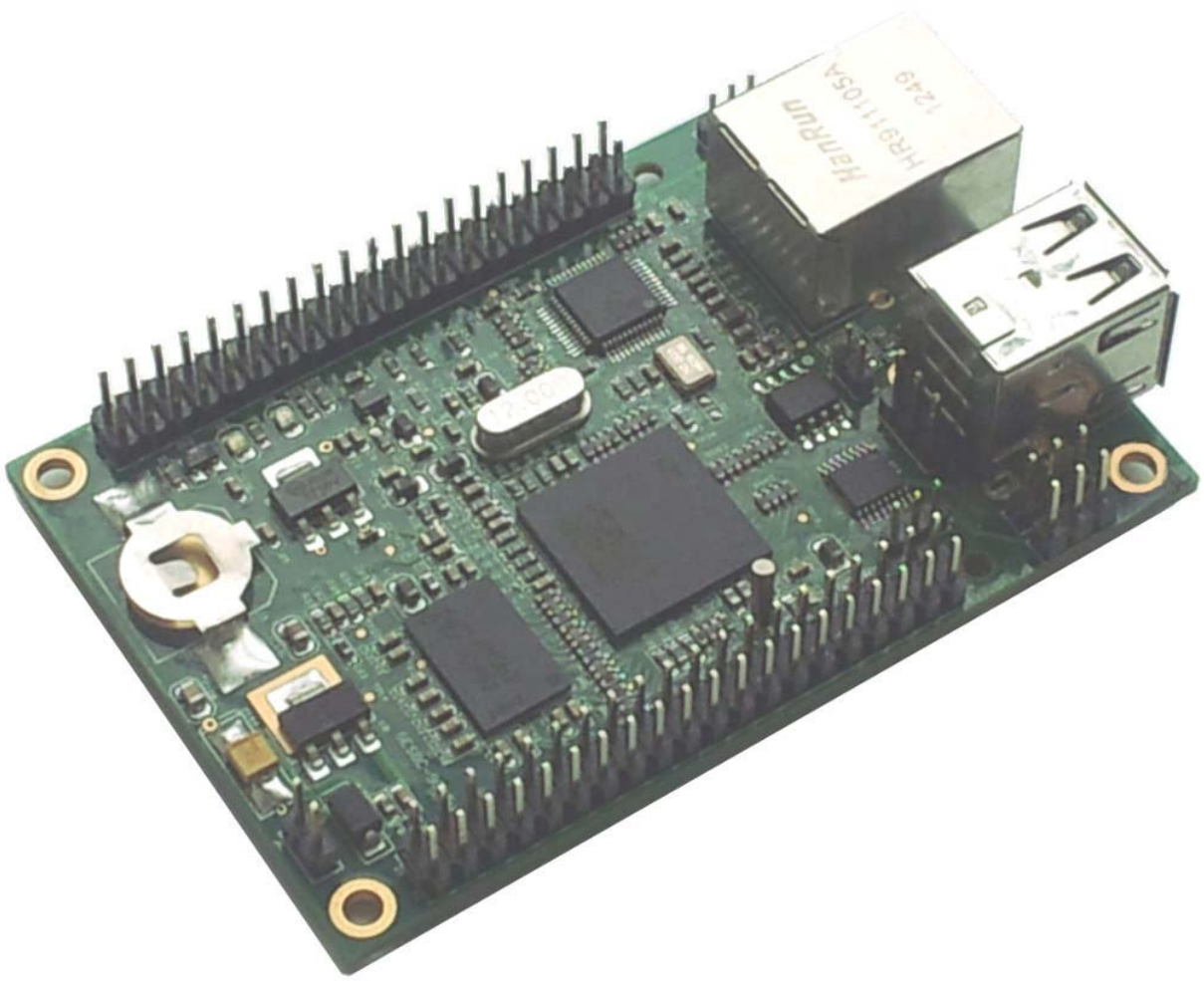

Figure 1. GESBC-9G25/35 Single Board Computer

Advanced Features

The heart of the GESBC-9G25/35 is the AT91SAM9G25/35 processor which is the one in a series of ARM926EJ-S-based processors. The AT91SAM9G25/35 microcontroller features DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration. It has separate 32 Kbyte instruction and data caches with write buffer. The ARM926EJ-S on the AT91SAM9G25/35 functions with a maximum operating clock rate of 400MHz and a power usage between 20mW and 80mW (dependent upon clock speed). The ARM core operates from a 1V supply while the I/O operates at 3.3V. The low power consumption makes it an idea platform for battery operated applications.

The list below summarizes the features of the GESBC-9G25/35.

- 400MHz Processor Core – ARM926EJ-S with MMU
- 128 MB DDR2RAM
- 128MB ~ 1GB NAND FLASH
- 1 10/100 Mbps Ethernet
- 12 channel 10-bit Analog-to-Digital Converter (ADC
- 4 Universal Asynchronous Receiver / Transmitters (UARTs)
- 2 USB Host Port
- 1 USB Device Port
- Real-Time Clock with Battery Backup
- Watchdog Timer
- Hardware Debug Interface
- Micro SD/MMC Socket
- I2C Port
- SPI Port
- TFT LCD controller (GESBC-9G35 only)

Chapter 2 – GESBC-9G25/35 Function Blocks

The GESBC-9G25/35 is designed as the heart of the system. It connects to the application specific carrier board through the SODIMM 200 interface. It consists of the processor and external memory and the board itself servers as a minimal CPU sub-system. The signals of a full suite of peripheral functions, such as USB, SD/MMC, I2C, I2S, Ethernet, etc, are routed to the SODIMM connector to be passed to the application specific carrier board. The following diagram shows the board architecture.

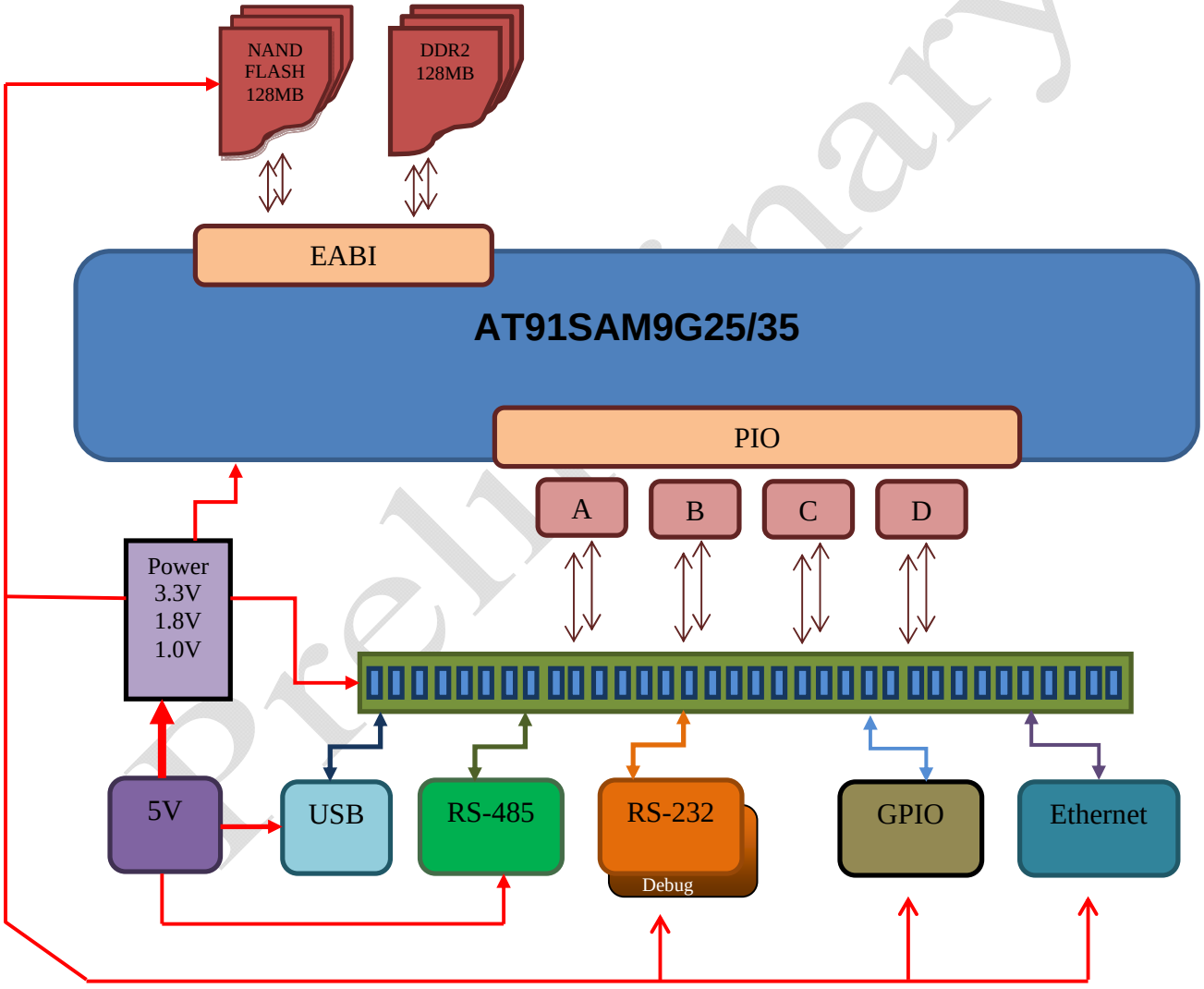

Figure 2. GESBC-9G25/35 Block Diagram

AT91SAM9G25/35

The GESBC-9G25/35 Single Board Computer uses the Atmel AT91SAM9G25/35 as the core processor on the computer module. The top-level features of AT91SAM9G25 processor are the following:

- ARM926EJ-S RISC Core Processor
- 400 MHz / 400 MIPS Performance
- 16Kbyte Instruction Cache
- 16Kbyte Data Cache
- Linux and Windows CE enabled MMU
- 133 MHz System Bus
- 32 bit External Bus Interface Supporting 8-banks DDR2/LPDDR, SDR/LPSDR, Static Memory
- MLC/SLC NAND Controller, with up to 24bit Programmable Multi-bit Error Correcting Code (PMECC)
- Serial EEPROM Interface
- 10 / 100 Mbps Ethernet MAC
- USB High Speed Host Port, USB Full Speed Host Port, USB High Speed Device Port
- Two High Speed Memory Card Hosts
- 4 UART
- Two-port USB Host (High Speed & Full Speed)
- 12 channel 10 bit ADC
- 2 Master/Slave SPI Port
- Serial Audio Interface
- TFT LCD Controller (AT91SAM9G35 only)
- JTAG Interface

More detailed information regarding the AT91SAM9G25/35 processor can be found at www.atmel.com.

DDR2 RAM

The GESBC-9G25/35 is equipped with 128MByte of DDR2RAM (double data rate synchronous dynamic memory). With the system clock running at 133MHz it can achieve a maximum transfer rate of ~ 1066 MB/S.

FLASH

The GESBC-9G25/35 is shipped with 128 Mbytes of NAND FLASH memory. The GESBC-9G25/35 can be also ordered with optional 256MB ~ 1GB NAND FLASH.

Ethernet

The GESBC-9G25/35 is shipped with a complete physical and MAC subsystem that is compliant with the ISO/TEC 802.3 topology for a single shared medium with several stations. The AT91SAM9G20/35 supports 1/10/100 Mbps transfer rates and interfaces to industry standard physical layer devices.

USB

The GESBC-9G25/35 is shipped with two USB host ports and one USB device port. The USB host ports are standard USB type A host port on a double stack USB host connector. The USB device port is on a 4 pin 2.54mm pitch male header.

Table 1 USB Device Port Connector J17

Pin Number	Signal Name
1	VUSB
2	-D
3	+D
4	GND

UART 1

The GESBC-9G25/35 is shipped with the 3 wire UART 1 interface.

Table 2 UART1 Port P1 Connector

Pin Number	Signal Name
1	RX
2	TX
3	GND

DEBUG Serial Port

The GESBC-9G25/35 is shipped with the 3 wire serial debug port.

Table 3 UART Port P0 Connector on GESBC-9G25/35

Pin Number	Signal Name
1	RX
2	TX
3	GND

RS-485[1]

The GESBC-9G25 Single Board Computer provides one half duplex RS-485 port. The RS-485 port is connected to USART3 with RTS signal for RS-485 driver direction control. The RS-485 signal is provided via a 1x3 2.54mm spacing header P2. J6 enables the on-board 120 ohm termination resistor.

Table 4 RS-485 Port P2

Pin Number	Signal Name
1	A
2	B
3	GND

The RTC3 is connected to the RS-485 driver chip for data direction control. The normal setting of RTS signal is normally low. For RS-485 mode the RTS signal must set to normally high. The user program must set the RTS mode before RS-485 port can be used.

RTC

The GESBC-9G25/35 uses the AT91SAM9G25/35 on-chip RTC with a coin cell battery holder to provide accurate time keeping. The on-board battery holder accepts CR1225/CR1220 coin cell batteries.

SPI, I2C, Additional USART, On-chip A/D, LCD Controller[2], and GPIO

The AT91SAM9G20 contains very rich set of peripherals that are multiplex into 3 groups, Peripheral A, Peripheral B, and Peripheral C, with individually programmable pins. The SPI bus, I2C, A/D and GPIO are provided together with other functions on the I/O expansion ports. The I/O expansion ports on the GESBC-9G25/35 are two 2x20 2.54mm spacing headers. The following tables list signals available on the I/O expansion connectors with their corresponding multiplexed functions and default usage on the GESBC-9G25/35 Single Board Computer.

Table 5 J21 I/O Expansion Connector 1

Pin	I/O Line	Peripheral A	Peripheral B	Peripheral C	On Board Function
1					0, +3.3V, or +5V via JP31
2					0, +3.3V, or +5V via JP31
3	PA0	TXD0	SPI1_NPCS1		
4	PA1	RXD0	SPI0_NPCS2		
5	PA2	RTS0	MCI1_DA1	ETX0	
6	PA3	CTS0	MCI1_DA2	ETX1	
7	PA4	SCK0	MCI1_DA3		
8	PA5	TXD1			UART1 TX
9	PA6	RXD1			UART1 RX
10	PA7	TXD2	SPI0_NPCS1		

[1] GESBC-9G25 only.
[2] LCD controller is only available on GESBC-9G35

11	PA8	RXD2	SPI1_NPCS0		
12	PA9	DRXD			Debug RX
13	PA10	DTXD			Debug TX
14	PA11	SPI0_MISO	MCI1_DA0		
15	PA12	SPI0_MOSI	MCI1_CDA		
16	PA13	SPI0_SPCK	MCI1_CK		
17	PA14	SPI0_NPCS0			
18	PA21	TIOA0	SPI1_MISO		
19	PA22	TIOA1	SPI1_MOSI		
20	PA23	TIOA2	SPI1_SPCK		
21	PA24	TCLK0	TK		
22	PA25	TCLK1	TF		
23	PA26	TCLK2	TD		
24	PA27	TIOB0	RD		
25	PA28	TIOB1	RK		
26	PA29	TIOB2	RF		
27	PA30	TWD0	SPI1_NPCS3	EMDC	
28	PA31	TWCK0	SPI1_NPCS2	ETXEN	
29	PB11	AD0		PWM0	
30	PB12	AD1		PWM1	
31	PB13	AD2		PWM2	
32	PB14	AD3		PWM3	
33	PB15	AD4			
34	PB16	AD5			
35	PB17	AD6			
36	PB18		IRQ	ADTRG	
37	PD14		D24		
38	PD16		D26	A23	
39					GND
40					GND

Table 6 J22 I/O Expansion Connector 2[3]

Pin	I/O Line	Peripheral A	Peripheral B	Peripheral C	Function
1					0, +3.3V, or +5V via JP32
2					0, +3.3V, or +5V via JP32
3	PC0		LCDDAT0	TWD1	
4	PC1		LCDDAT1	TWCK1	
5	PC2		LCDDAT2	TIOA3	
6	PC3		LCDDAT3	TIOB3	
7	PC4		LCDDAT4	TCLK3	
8	PC5		LCDDAT5	TIOA4	

[3] The peripheral B block function on J22 lists AT91SAM0G35 peripherals. For AT91SAM9G25 peripherals please reference AT91SAM9G25 data sheet.

9	PC6		LCDDAT6	TIOB4	
10	PC7		LCDDAT7	TCLK4	
11	PC8		LCDDAT8	UTXD0	
12	PC9		LCDDAT9	URXD0	
13	PC10		LCDDAT10	PWM0	
14	PC11		LCDDAT11	PWM1	
15	PC12		LCDDAT12	TIOA5	
16	PC13		LCDDAT13	TIOB5	
17	PC14		LCDDAT14	TCLK5	
18	PC15		LCDDAT15	PCK0	
19	PC16		LCDDAT16	UTXD1	
20	PC17		LCDDAT17	URXD1	
21	PC18		LCDDAT18	PWM0	
22	PC19		LCDDAT19	PWM1	
23	PC20		LCDDAT20	PWM2	
24	PC21		LCDDAT21	PWM3	
25	PC22		LCDDAT22		
26	PC23		LCDDAT23		
27	PC24		LCDDISP		
28	PC25				
29	PC26		LCDPWM		
30	PC27		LCDVSYNC	RTS1	
31	PC28		LCDHSYNC	CTS1	
32	PC29		LCDEN	SCK1	
33	PC30		LCDPCK		
34	PC31		FIQ	PCK1	
35	PD17	D27	A24		
36	PD18	D28	A25		
37	PD19	D29	NCS2		
38	PD20	D30	NCS4		
39					GND
40					GND

JTAG

The GESBC-9G25/35 Single Board Computer is shipped with a 2x5 2.54mm pitch SMT header footprint that provides JTAG debug signals for the CPU. The JTAG provides the user with the ability to debug system level programs. The signal designation is listed in the following table.

Table 7 J20 JTAG Connector

Pin Number	Signal Name	Pin Number	Signal Name
1	3.3V	2	3.3V
3	NTRST	4	TDI
5	TMS	6	TCK
7	RTCK	8	TDO

9	GND	10	GND

Power Requirement

The GESBC-9G25/35 Single Board Computer requires regulated 5V DC. The power supply should have minimum 300mA capacity.

Table 8 J1 Power Supply Connector

Pin Number	Signal Name
1	+5V DC
2	GND

Chapter 3 – Software Description

Overview

This chapter provides information regarding the software that is shipped with the GESBC-9G25/35 Board. The software included with the board includes U-Boot boot loader, Linux kernel 2.6.39, and an embedded root file system.

Data Storage on GESBC-9G25/35

The default configuration of the GESBC-9G25/35 Single Board Computer uses on board NAND FLASH for all data storage requirements, including boot strap code, boot loader, Linux kernel, and Linux file system.

The following table is the factory default storage map on the NAND FLASH.

Table 9 NAND FLASH Storage Map

Start Address	Size	Usage
0x00000000	0x20000	Boot strap code
0x00040000	0x40000	U-Boot
0x000C0000	0x20000	U-Boot primary environment storage range
0x000E0000	0x20000	U-Boot secondary environment storage range
0x00200000	0x300000	Linux kernel
0x00800000	--	Root file system

GESBC-9G25/35 Linux Code

The GESBC-9G25/35 is shipped with Linux 2.6.39 kernel pre-installed. This software is programmed in the system FLASH located on the board prior to shipment. The Linux kernel is configured with most of the device drivers included for the GESBC-9G25/35 board.

U-boot

U-Boot provides a simple interface for loading operating systems and applications onto the GESBC-9G25/35 board. U-Boot uses a serial console for its input and output. The default serial port setting is 115200,8,N,1. It also supports the built-in Ethernet port and general flash programming.

The board is shipped with U-Boot pre-installed. Please refer to U-Boot user's manual regarding detailed information of U-Boot.

U-Boot Booting Linux

The following shows the default U-Boot setup for booting Linux.

```
U-Boot> printenv
bootargs=mem=128M console=ttyS0,115200 mtdparts=atmel_nand
8M(bootstrap/uboot/kernel)ro,-(rootfs) root=/dev/mtdblock1 rw
rootfstype=ubifs ubi.mtd=1 root=ubi0:rootfs
bootdelay=1
baudrate=115200
ethaddr=00:0c:20:02:0a:5b
ipaddr=192.168.0.200
serverip=192.168.0.102
netmask=255.255.255.0
stdin=serial
stdout=serial
stderr=serial
ethact=macb0

Environment size: 353/131067 bytes
U-Boot>
```

The `bootcmd` setting of the U-Boot reads the Linux kernel from NAND FLASH at address 0x200000 to SDRAM at address 0x22000000 and start executing the kernel code at the same memory address. The NAND FLASH from 0x800000 and up is used for Linux root file system. The U-Boot passes the MTD device partition setting to the Linux kernel via the `bootargs` environment variable.

Loading Linux Kernel and root File System

The U-Boot boot-loader provides many ways to load Linux kernel and file system into FLASH memory. The loading by Ethernet network is shown here. User can consult U-Boot manual for other methods of loading data.

After power on the GESBC-9G25/35 board, stop the U-boot auto-execution by press any key. The following message should be shown on the terminal console on the host PC connected to the GESBC-9G25/35 board.

```
RomBOOT
Start AT91Bootstrap...
Init DDR...  ba_offset = 0xb ... Done!
Loading 1-Wire info...
Enumerate all roms:
Rom#0x0: 0xa3 0x0 0x0 0x3 0x21 0x88 0x63 0x2d
Done, 0x1 1-wire chips found!

Board name: SAM9x5-EK [B0]; Vendor name: FLEX
sn: 0x4000023;   rev: 0x8401
Downloading image...
chip id: 0xecda
Copy 0x50000 bytes from 0x40000 to 0x26f00000
Done!


U-Boot 2010.06 (Jun 23 2011 - 16:05:54)

DRAM:  128 MiB
NAND:  256 MiB
```

The network address and server address must be set before network transfer can take place. The following commands will set the SBC IP address and server IP address,

```
set ipaddr xxx.xxx.xxx.xxx
set serverip xxx.xxx.xxx.xxx
```

The server IP is the IP address where a TFTP server must be run. To load Linux kernel type in the following command,

```
tftp 0x22000000 uImage
```

The U-Boot will load uImage file from the TFTP server whose IP address is specified by the `serverip` environment variable.

The NAND FLASH sectors must be erased first before new kernel image can be stored. The following command will erase the NAND FLASH sectors reserved for Linux kernel,

```
nand erase 0x200000 0x280000
```

The use the flowing command to store the kernel image from SDRAM to NAND FLASH,

```
nand write.jffs2 0x22000000 0x200000 0x280000
```

The following commands can be used to load root file system into the FLASH memory,

```
nand erase 0x800000 [available_nand_flash_memory_size]
tftp 0x21000000 rootfs.img
nand write.jffs2 0x21000000 0x800000 $(filesize)
```

Please be noted that the image is first loaded into the SDRAM and then stored into the FLASH memory. The image size can not exceed the available SDRAM on the board.

After the kernel and root file system have been updated the board can be simply reboot by recycle the power.

Chapter 4 – Development Tools

Glomation provides a pre-configured VMWare image based Linux Debian distribution that includes cross development tool chain, Eclipse IDE, sample project and sample program. The user and password pairs for the VMWare image are root:root and user:user. The VMWare image is available in the support page at Glomation website, http://www.glomationinc.com/support.html