Glomation

Embedded CPU Module

GECM-5100

User's Manual

Table of Contents

List of Tables

Chapter 1 – Introducing the GECM-5100 CPU Module

GECM-5100 Overview

The GECM-5100 is a low cost compact sized CPU Module based on Atmel SAMA5D3 series processors. It integrates all the core components and is mounted onto an application-specific carrier board using the standard SODIMM form factor. This approach allows the customer to design a customer carrier board that meets the customer's I/O, dimensional, and connector requirements without having to go through complicated design process of the processor, memory, and standard I/O functionality. It can significantly reduce the development time and simplifying the process of developing a complete customer product. With a large peripheral set targeted to a variety of applications, the GECM-5100 is well suited for industrial controls, digital media servers, audio jukeboxes, thin clients, set-top boxes, point-of-sale terminals, biometric security systems, and GPS devices.

Figure 1. GECM-5100 CPU Module

Advanced Features

The heart of the GECM-5100 is the SAMA5D3 series of ARM® Cortex®-A5 processors. The SAMA5D3 series high-performance, power-efficient embedded MPU features a floating point unit for high-precision computing and accelerated data processing, and a high data bandwidth architecture. It integrates advanced user interface and connectivity peripherals and security features. The SAMA5D3 series features an internal multi-layer bus architecture associated with 39 DMA channels to sustain the high bandwidth required by the

processor and the high-speed peripherals. The device offers support for DDR2/LPDDR/LPDDR2 and MLC NAND Flash memory with 24-bit ECC. The comprehensive peripheral set includes an LCD controller with overlays for hardware-accelerated image composition, a touch screen interface and a CMOS sensor interface. Connectivity peripherals include Gigabit EMAC with IEEE1588, 10/100 EMAC, multiple CAN, UART, SPI and I2C. With its secure boot mechanism, hardware accelerated engines for encryption (AES, TDES) and hash function (SHA), the SAMA5D3 ensures anti-cloning, code protection and secure external data transfers. The SAMA5D3 series is optimized for control panel/HMI applications and applications that require high levels of connectivity in the industrial and consumer markets. Its low power consumption levels make the SAMA5D3 particularly suited for battery-powered devices.

The list below summarizes the features of the GECM-5100.

- 536MHz Processor Core – ARM® Cortex®-A5
- 256 MB DDR2RAM
- 256MB ~ 1GB NAND FLASH
- 1 GigaBit Ethernet MAC
- 12 channel 10-bit Analog-to-Digital Converter (ADC
- 4 Universal Asynchronous Receiver / Transmitters (UARTs)
- 2 USB Host Port
- 1 USB Device Port
- Real-Time Clock
- Watchdog Timer
- Hardware Debug Interface
- SD/MMC Interface
- I2C Port
- SPI Port

Chapter 2 – GECM-5100 Function Blocks

The GECM-5100 is designed as the heart of the system. It connects to the application specific carrier board through the SODIMM 200 interface. It consists of the processor, external memory, and GigaBit Ethernet. The signals of a comprehensive set of peripheral functions, such as USB, SD/MMC, I2C, I2S, Ethernet, etc, are routed to the SODIMM connector to be passed to the application specific carrier board. The following diagram shows the board architecture.

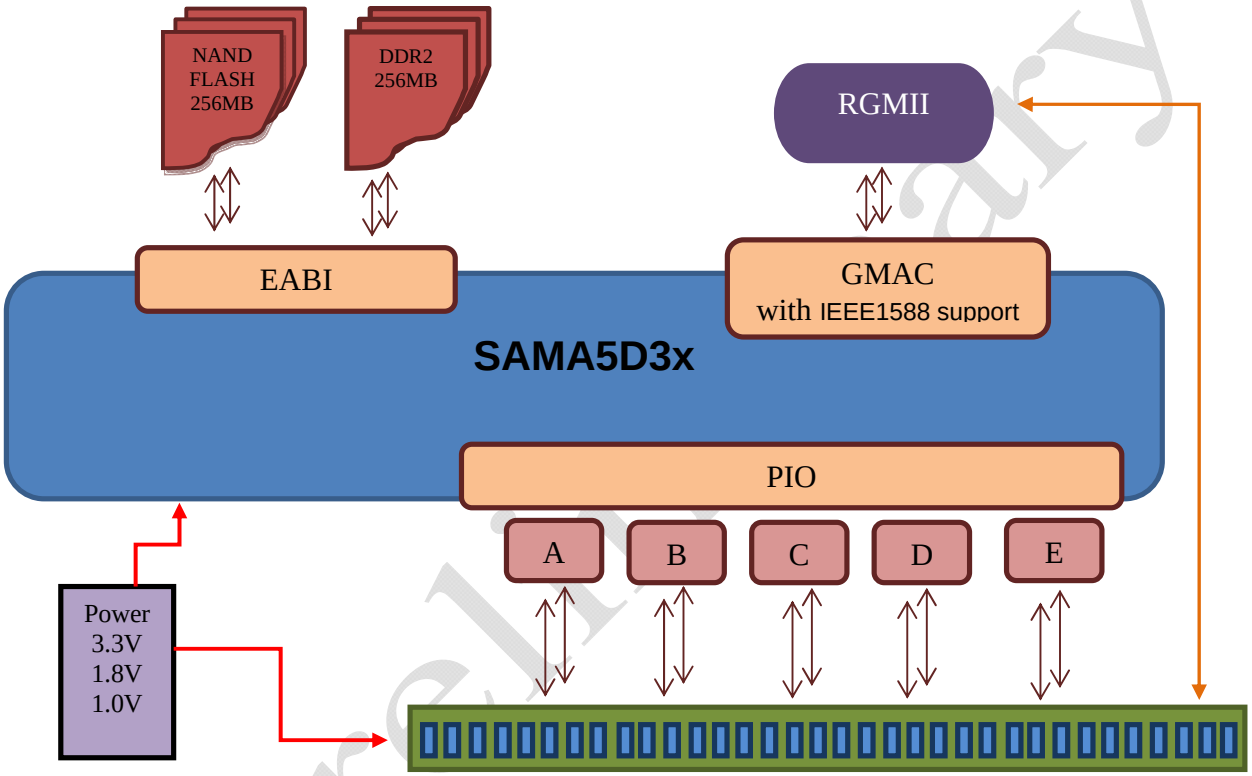

Figure 1. GECM-5100 Block Diagram

SAMA5D3X

The GECM-5100 CPU Module uses the Atmel SAMA5D3X as the core processor on the computer module. The top-level features of SAMA5D3X processor are the following:

- ARM® Cortex®-A5 Processor with ARM v7-A Thumb2® Instruction Set
- 536 MHz Performance
- 32Kbyte Instruction Cache
- 32Kbyte Data Cache

- Fully Integrated MMU and Floating Point Unit (VFPv4)
- System Running up to 166 MHz
- High Bandwidth 32 bit Multi-port Dynamic RAM Controller Supporting 512MByte 8-banks DDR2/LPDDR/LPDDR2
- MLC/SLC NAND Controller, with up to 24bit Programmable Multi-bit Error Correcting Code (PMECC)
- Serial EEPROM Interface
- 10/100/1000 Mbps Gigabit Ethernet MAC with IEEE 1588 support
- LCD TFT Controller with Overlay. Alpha-blending, Rotation, Scaling, and Color Space Conversion
- Three High Speed/Full Speed/Low Speed USB Transceivers
- Three High Speed Memory Card Hosts (eMMC 4.3 and SD 2.0)
- 4 USART, 2 UART, one DBGU
- 2 CAN Controllers
- 12 channel 10 bit ADC
- 2 Master/Slave SPI Port
- Serial Audio Interface
- Up to 160 GPIOs
- JTAG Interface

More detailed information regarding the SAMA5D3 processors can be found at www.atmel.com.

DDR2 RAM

The GECM-5100 is equipped with 256MByte of DDR2RAM (double data rate synchronous dynamic memory). The GECM-5100 can be also ordered with optional 512MB DDR2RAM.

FLASH

The GECM-5100 is shipped with 256 Mbytes of NAND FLASH memory. The GECM-5100 can be also ordered with optional 512MB ~ 1GB NAND FLASH.

Clock Circuitry

The GECM-5100 CPU Module includes tow clock sources, 32.768KHz crystal for RTC and 12MHz crystal for main system clock.

Reset Circuitry

The reset sources for the GECM-5100 are,

- Power on reset
- Push button reset (from carrier board)
- JTAG reset from an in-circuit emulator (option JTAG interface on carrier board)

Power Supply

The GECM-5100 CPU Module contains its own power supply generation circuit to generate necessary power source for the processor and main memory. Additional power source for other peripheral functions should be provided by carrier board to the CPU module through the SODIMM interface. The following table lists the power source and functionality.

Table 1 Power Sources

Nominal	Name	Powers	Source
3.3V	VDDNF	NAND Flash and D16 ~ D32 Multiplex SMC Data Lines	Derived from 3.3V From SODIMM connector. Output to the SODIMM as VDDNF for carrier board voltage shifter (if needed).
3.3V	VDDIOP0	Partial Peripheral I/O lines	From SODIMM connector
3.3V	VDDIOP1	Partial Peripheral I/O lines	From SODIMM connector
3.0V	VDDBU	The Slow Clock Oscillator, the 32KHz RC, the Internal 12MHz RC and Part of the System Controller	From SODIMM connector
3.3V	VDDUTMII	The USB Device and Host UTMII+ Interface	From SODIMM connector
3.3V	VDDOSC	The Main Oscillator Cell	From SODIMM connector
3.3V	VDDANA	The Analog to Digital Converter	From SODIMM connector
1.8V	VDDIOM	The External Memory Interface	On-board Power Supply
1.0V	VDDUTMIC	DC Supply UDPHS and UHPHS UTMI+ Core	On-board Power Supply
3.3V	VDDPLLUTMI	DC Supply UDPHS and UHPHS UTMI interface	From SODIMM connector
1.0V	VDDPLLA	The PLLA Cell	From SODIMM connector
1.0V	VDDCORE	CPU Core Power Supply	On-board Power Supply
3.0V/3.3V	ADVREF	ADC Reference voltage	From SODIMM connector

SODIMM 200 Interface

The GECM-5100 CPU Module uses SODIMM card edge connector to interface the application specific carrier board. Table 2 shows the pin assignment and multiplexed peripheral functions if applicable. The

PIO function block A, B, and C are integrated peripheral function blocks on the processor. Please see SAMA5Dx processor data sheet for detailed information on the multiplexed peripheral functions.

Table 2 J1 SODIMM 200 Card Edge Connector

PIO C	PIO B	PIO A		SODIMM 200			PIO A	PIO B	PIO C
Front Side				A		B	Back Side		
VCC 5V				1		2	VCC 5V		
VCC 5V				3		4	VCC 5V		
GND				5		6	VBAT		
		CTS2	PE23	7		8	PE29	NWR1/NBS1	TCLK2	
		RTS2	PE24	9		10	PE30	NWAIT		
		RXD2	PE25	11		12	PE31	TRQ	PWML1	
		TXD2	PE26	13		14	GND			
VDDIOM				15		16	VDDIOM			
		SPI1_NPCS0	PC25	17		18	PC24	SPI1_SPCK		
		SPI_MOSI	PC23	19		20	PC22	SPI1_MISO		
		RD0	PC21	21		22	PC20	RF0		
GND				23		24	PC19	RK0		
		TD0	PC18	25		26	PC17	TF0		
		TK0	PC16	27		28	PC9	EMDIO	PIO	
	TCLK5	EMDC	PC8	29		30	PC7	EREFCK	TIOB5	
	TIOA5	ERXER	PC6	31		32	GND			
	TIOB4	ETXEN	PC4	33		34	PC5			
	TCLK3	ERX0	PC2	35		36	PC3			
	TIOA3	ETX0	PC0	37		38	PC1			
			ENABLE_0	39		40	ENABLE_1	CS Boot Disable		
				Key						
VCC 3V3				41		42	VCC 3V3			
VCC 3V3				43		44	VCC 3V3			
ENABLE_2				45		46	ENABLE_3			
NC				47		48	ADDVREF			
LCDDAT22	TIOA2	NCS1	PE27	49		50	PE28	NCS2	TIOB2	LCDDAT23
	LCDDAT20	MCI2_CDA	PC10	51		52	PC11	MCI2_DA0	LCDDAT19	PIO
GND				53		54	PC13	MCI2_DA2	TIOB1	LCDDAT17
LCDDAT18	TIOA1	MCI2_DA1	PC12	55		56	PC15	MCI2_CK	PCK2	LCDDAT21
LCDDAT16	TCLK1	MCI2_DA3	PC14	57		58	PC26	SPI1_NPCS1		ISI_D11
ISI_D10		SPI1_NPCS2	PC27	59		60	PC28	SPS1_NPCS3	PWMF10	ISI_D9
ISI_D8	PWMFI2	URXD0	PC29	61		62	GND			
	PWMFI1	FIQ	PC31	63		64	PC30	UTXD0	ISI_PCK	
VDDIOP0				65		66	VDDIOP0			
		LCDDAT0	PA0	67		68	PA1	LCDDAT1		
		LCDDAT2	PA2	69		70	PA3	LCDDAT3		
GND				71		72	PA4	LCDDAT4		
		LCDDAT5	PA5	73		74	PA6	LCDDAT6		
		LCDDAT7	PA7	75		76	PA8	LCDDAT8		
		LCDDAT9	PA9	77		78	PA10	LCDDAT10		
		LCDDAT11	PA11	79		80	GND			
		LCDDAT12	PA12	81		82	PA13	LCDDAT13		
		LCDDAT14	PA14	83		84	PA15	LCDDAT15		
	ISI_D0	LCDDAT16	PA16	85		86	PA17	LCDDAT17	ISI_D1	
ISI_D2	TWD2	LCDDAT18	PA18	87		88	PA19	LCDDAT19	TWCK2	ISI_D3
GND				89		90	PA20	LCDDAT20	PWMH0	ISI_D4
ISI_D5	PWML0	LCDDAT21	PA21	91		92	PA22	LCDDAT22	PWMH0	ISI_D6
ISI_D7	PWML1	LCDDAT23	PA23	93		94	PA24	LCDPWM		
		LCDDISP	PA25	95		96	PA26	LCDVSYNC		
		LCDHSYNC	PA27	97		98	GND			
ISI_VSYNC	URXD1	LCDPCK	PA28	99		100	LCDDEN			
		TWD0	PA30	101		102	TWCK0	UTXD1	ISI_HSYNC	
VDDANA				103		104	VDDANA			
	PCK0	AD10	PD30	105		106	PD31	AD11	PCK1	
GND				107		108	PD29	AD9		
		AD8	PD28	109		110	PD27	AD7		
		AD6	PD26	111		112	PD25	AD5		
		AD4	PD24	113		114	PD23	AD3		

		AD2	PD22	115		116	GND			
		AD0	PD20	117		118	PD21	AD1		
		TXD0	PD18	119		120	PD19	ADTRG		
PWMF13	SPI-_NPCS3	RTS0	PD16	121		122	PD17	RXD0	PIO	
CANRX0	SPI0_NPCS1	SCK0	PD14	123		124	PD15	CTS0	SPI0_NPCS2	CANTX0
GND				125		126	PD13	SPI0_NPCS0		
		SPI0_SPCK	PD12	127		128	PD11	SPI0_MOSI		
		SPI0_MISO	PD10	129		130	PD9	MCI0_CK		
PIO	PWML3	MCI0_DA7	PD8	131		132	PD7	MCI0DA6	TCLK0	PWMH3
PWML2	TIOB0	MCI0_DA5	PD6	133		134	GND			
PWMH2	TIOA0	MCI0_DA4	PD5	135		136	PD4	MCI0_DA3		
		MCI0_DA2	PD3	137		138	PD2	MCI0_DA1		
		MCI0_DA0	PD1	139		140	PD0	MCI0_CDA		
VDDIOP1				141		142	VDDIOP1			
GND				143		144	PB13	GRXER	PWML3	
	EF1	GTXER	PB10	145		146	PB12	GRXDV	PWMH3	
	CANRX1	GCRS	PB14	147		148	PB15	GCOL	CANTX1	
	GTX4	MCI1_CDA	PB19	149		150	PB20	MCI1_DA0	GTX5	
	GTX6	MCI1_DA1	PB21	151		152	PB22	MCI1_DA2	GTX7	
	GRX4	MCI1_DA3	PB23	153		154	GND			
	GRX5	MCI1_CK	PB24	155		156	PB25	SCK1	GRX6	
GND				157		158	PB27	RTS1	PWMH1	
			USBA_DP	159		160	PB29	TXD1	PIO	
			USBA_DM	161		162	PB31	DTXD		
GND				163		164	PB30	DRXD		
			USBB_DP	165		166	PB26	CTS1	GRX7	
			USBB_DM	167		168	PB28	RXD1	PIO	
GND				169		170	GND			
			USBC_DP	171		172	DIBP			
			USBC_DM	173		174	DIBN			
GND_ETH				175		176	GND			
			ETH0_TX1+	177		178	JTAGSEL		SYSC	
			ETH0_TX1-	179		180	WKUP		SYSC	
			ETH0_RX1+	181		182	SHDN		SYSC	
			ETH0_RX1-	183		184	BMS		RSTJTAG	
GND_ETH				185		186	nRST		SYSC	
			ETH0_TX2+	187		188	nTRST		RSTJTAG	
			ETH0_TX2-	189		190	TDI		RSTJTAG	
			ETH0_RX2+	191		192	TCK		RSTJTAG	
			ETH0_RX2-	193		194	TMS		RSTJTAG	
GND				195		196	TDO		RSTJTAG	
			LED2	197		198	RTCK		RSTJTAG	
			LED1	199		200	GND			

Connector

The GECM-5100 CPU Module uses SODIMM card edge connector to interface the carrier board. The board dimensions is shown below.

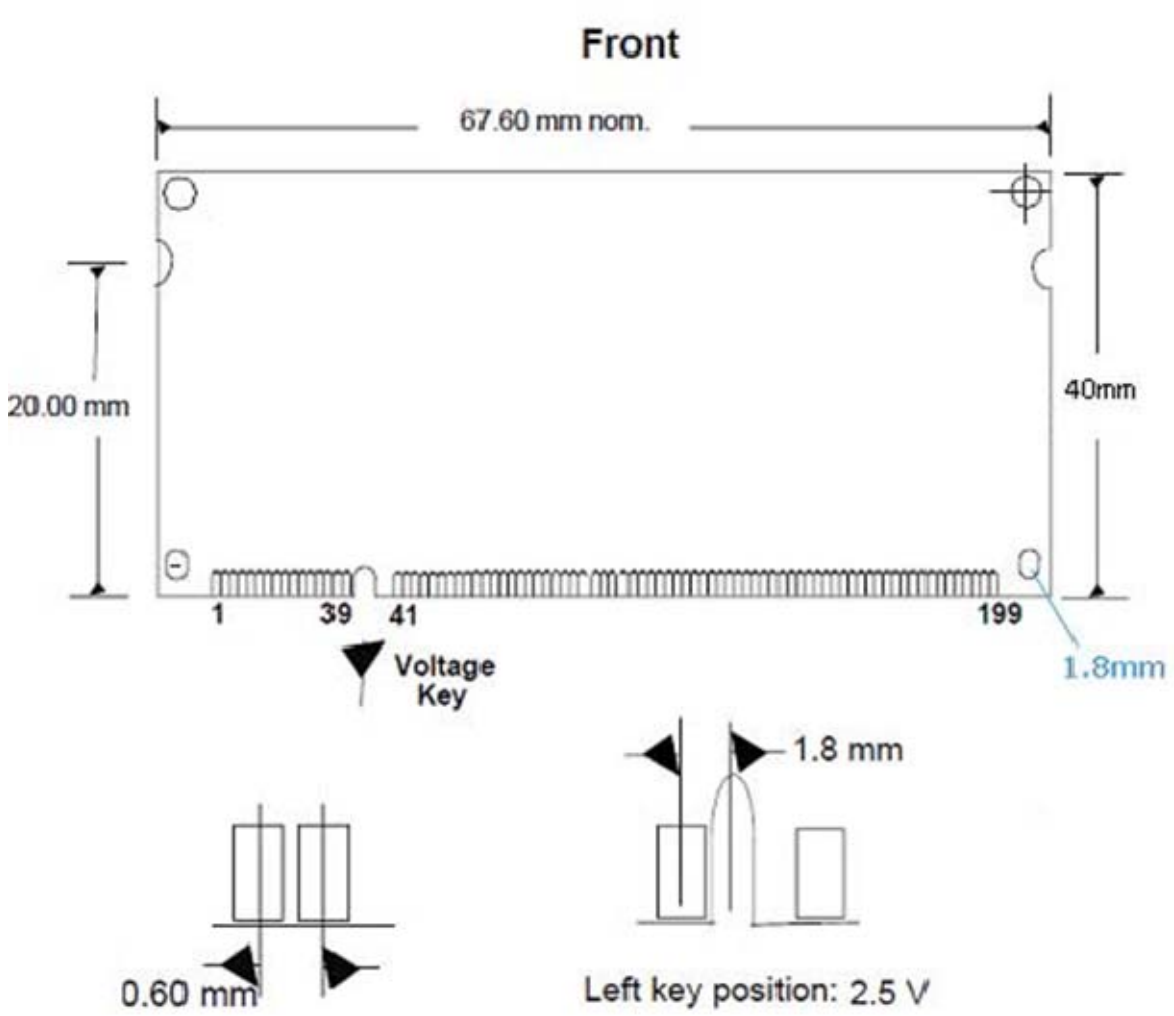

Figure 1. SODIMM 200 Dimensions

Chapter 3 – Software Description

Overview

This chapter provides information regarding the software that is shipped with the GECM-5100 Board. The software included with the board is U-Boot boot loader, Linux kernel 2.6.39, and an embedded root file system.

Data Storage on GECM-5100

The default configuration of the GECM-5100 CPU Module uses on board NAND FLASH for all data storage requirements, including boot strap code, boot loader, Linux kernel, and Linux file system.

The following table is the factory default storage map on the NAND FLASH.

Table 3 NAND FLASH Storage Map

Start Address	Size	Usage
0x00000000	0x20000	Boot strap code
0x00040000	0x40000	U-Boot
0x000C0000	0x20000	U-Boot environment storage
0x00180000	0x20000	Kernel device tree data storage
0x00200000	0x600000	Linux kernel
0x00800000	--	Root file system

GECM-5100 Linux Code

The GECM-5100 is shipped with Linux 2.6.39 kernel pre-installed. This software is programmed into the system FLASH located on the board prior to shipment. The Linux kernel is configured with most of the device drivers included for the GECM-5100 board.

U-boot

U-Boot provides a simple interface for loading operating systems and applications onto the GECM-5100 board. U-Boot uses a serial console for its input and output. The default serial port setting is 115200,8,N,1. It also supports the built-in Ethernet port and general flash programming.

The board is shipped with U-Boot pre-installed. Please refer to U-Boot user's manual regarding detailed information of U-Boot.

U-Boot Booting Linux

The following shows the default U-Boot setup for booting Linux.

```
U-Boot 2013.04 (Jul 06 2013 - 07:32:33)

CPU: SAMA5D34
Crystal frequency:       12 MHz
CPU clock        :      528 MHz
Master clock     :      132 MHz
DRAM:  512 MiB
NAND:  256 MiB
MMC:   mci: 0
In:    serial
Out:   serial
Err:   serial
Net:   No ethernet found.
Hit any key to stop autoboot:  0

NAND read: device 0 offset 0x180000, size 0x50f3
 20723 bytes read: OK

NAND read: device 0 offset 0x200000, size 0x2b3dd8
 2833880 bytes read: OK
```

The `bootcmd` setting of the U-Boot reads the Linux kernel from NAND FLASH at address 0x200000 to SDRAM at address 0x22000000 and start executing the kernel code at the same memory address. The NAND FLASH from 0x800000 and up is used for Linux root file system. The U-Boot passes the MTD device partition setting to the Linux kernel via the `bootargs` environment variable.

Loading Linux Kernel and root File System

The U-Boot boot-loader provides many ways to load Linux kernel and file system into FLASH memory. The loading by Ethernet network is shown here. User can consult U-Boot manual for other methods of loading data.

After power on the GECM-5100 board, stop the U-boot auto-execution by press any key. The following message should be shown on the terminal console on the host PC connected to the GECM-5100 board.

```
RomBOOT


AT91Bootstrap 3.5.3 (Mon Jul  8 14:08:30 EDT 2013)

1-Wire: Loading 1-Wire information ...
1-Wire: ROM Searching ... Done, 0x1 1-Wire chips found

1-Wire: BoardName | [Revid] | VendorName
WARNING: 1-Wire: Failed to get board information

1-Wire: Using defalt value SYS_GPBR2: 0x481242a, SYS_GPBR3:
0x6a0823

NAND: ONFI flash detected
NAND: Manufacturer ID: 0x2c Chip ID: 0x32
NAND: Disable On-Die ECC
NAND: Initialize PMECC params, cap: 0x4, sector: 0x200
NAND: Image: Copy 0x80000 bytes from 0x40000 to 0x26f00000
NAND: Done to load image
```

The network address and server address must be set before network transfer can take place. The following commands will set the SBC IP address and server IP address,

```
set ipaddr xxx.xxx.xxx.xxx
set serverip xxx.xxx.xxx.xxx
```

The server IP is the IP address where a TFTP server must be run. To load Linux kernel type in the following command,

```
tftp 0x22000000 uImage
```

The U-Boot will load uImage file from the TFTP server whose IP address is specified by the `serverip` environment variable.

The NAND FLASH sectors must be erased first before new kernel image can be stored. The following command will erase the NAND FLASH sectors reserved for Linux kernel,

```
nand erase 0x200000 0x200000
```

The use the flowing command to store the kernel image from SDRAM to NAND FLASH,

```
nand write 0x22000000 0x200000 0x200000
```

The following commands can be used to load root file system into the FLASH memory,

```
nand erase 0x800000 [available_nand_flash_memory_size]
tftp 0x20000000 rootfs.img
nand write.trimfs 0x20000000 0x800000 $(filesize)
```

Please be noted that the image is first loaded into the SDRAM and then stored into the FLASH memory. The image size can not exceed the available SDRAM on the board.

After the kernel and root file system have been updated the board can be simply reboot by recycle the power.